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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
FOTAKIS, ARISTOCRATIS	
ART UNIT	**PAPER NUMBER**
2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/800,653	SU ET AL.	
	Examiner	Art Unit	
	Aristocratis Fotakis	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1 and 11 are objected to because of the following informalities: The claims recite of an accumulated effect of the phase transition. However, according to the figures the phase transition data is encoded which has not been recited in lines 6 – 7 of claims 1 and 11. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 – 3, 5 – 7, 11 – 13 and 16 - 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,850,422).

Re claims 1 and 11, Chen teaches of a method and a system comprising: a clock for generating a clock signal (#12, Fig.1 and Fig.2, Col 3 Lines 59 – 67); a phase detector for oversampling the transmitted serial data and providing sampled data (#14, Fig.1, Col 4, Lines 35 – 45) and for detecting phase transitions between a phase lead and a phase lag (#18, Fig.1) in the sampled data and outputting phase transition data (#50, Fig.6A); an encoder for encoding the phase transition data (#52, combinational logic, Fig.6A, truth table, Fig.6B); a confidence counter (#20, Fig.1) coupled to receive the phase transition data (output from encoding in #18) and provide an output representative of an accumulated effect (Col 1, line 67 to Col 2, Lines 1 – 5) of the phase transitions (Col 6, Lines 36 – 67 and Col 7, Lines 1 - 19); and a phase selector

(#16, CLOCK MUX, Fig.1), coupled to receive the clock signal and the output from the confidence counter (#20), for selecting an optimum phase effective for recovering the clock relative to the transmitted serial data (Fig.4, Col 4, Lines 66 – 67 to Col 5, Lines 1 – 19 and Fig.1). However, Chen does not teach of a clock signal generated in half the rate of the transmitted serial data signal.

It would have been an obvious matter of design choice to generate the clock signal in half the rate of the transmitted serial data signal. Applicant has not disclosed that a clock signal generated in half the rate of the transmitted serial data signal provides an advantage or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicants invention to perform equally well with providing a clock of the same frequency as the data rate of the incoming data to reduce power consumption (Col 4, Lines 10 – 16).

Re claims 2 – 3 and 12 - 13, Chen teaches of the phase detector oversampling the transmitted serial data at ten times the rate of the transmitted serial data wherein the clock signal has ten phases for each period in the transmitted serial data.

Chen does not disclose of oversampling the transmitted data at four times the sampling rate wherein the clock signal has eight phases for each period in the transmitted serial data. It would have been an obvious matter of design choice to oversample the transmitted serial data at four times the rate of the transmitted serial data wherein the clock signal has ten phases for each period in the transmitted serial

data. Applicant has not disclosed that the 4Xoversampling rate wherein the clock signal has eight phases for each period in the transmitted serial data provides an advantage or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicants invention to perform equally well with providing the ten phase used for oversampling rate for better noise or jitter tolerance (Col 4, Lines 35 – 38).

Re claim 5, Chen teaches of the clock comprising a phase locked loop (#12, PLL, Fig.1 and Fig.2).

Re claim 6, Chen teaches of the confidence counter comprising a state machine (#20, Fig.1 and Fig.7) for identifying each of the detected phase leads and the detected phase lags (output from #18, Fig.1).

Re claims 7 and 17 - 18, Chen teaches of the state machine further comprises an initial state (move around *ideal position,* Col 6, Lines 45 - 51), ten states for each detection of the phase lead, and ten states for each detection of the phase lag (shifting left or right, Col 6, Lines 45 – 55). The number of states is the number of phases used. The number of phases was a designer's choice as discussed above.

Re claim 16, Chen teaches of a system comprising: a clock for generating an 8-phase clock signal at half rate of transmitted serial data (see claim 3); a half-rate phase detector for oversampling the transmitted serial data at four times the half clock rate and providing sampled data, and for detecting phase transitions between a phase lead and a phase lag in the sampled data and outputting phase transition data; a confidence counter coupled to receive the phase transition data and provide an output representative of an accumulated effect of the phase transitions; and a phase selector, coupled to receive the clock signal and the output from the confidence counter, for selecting an optimum phase effective for recovering the clock relative to the transmitted serial data (see claim 1).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Nakamura (US Pub 2002/0030522).

Chen teaches all the limitations of claim 1 except of the use of the clock comprising a DLL.

Nakamura teaches of an oversampling clock recovery circuit (title of invention) where a relatively small number of clocks are supplied, and controlled in phase by a phase control circuit. From the phase-controlled clocks, a delay-locked loop (DLL) generates a relatively large number of clocks (multiphase clocks) required for phase comparison, and supplies generated clocks to the phase comparators for phase comparison (Paragraph 0028).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a DLL to generate a relatively large number of clocks (multiphase clocks) required for phase comparison, and supply generated clocks to the phase comparators for phase comparison.

Claims 8 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Huang et al (US 7,113,560).

Re claims 8 and 19, Chen teaches all the limitations of claims 1 and 16, except of a state machine having four states for shifting the sampling phase toward the optimum phase.

Huang teaches of a method and circuit to produce an optimal sampling phase for recovery of a digital signal. A digital signal is *over-sampled* by sampling on each phase of a *multiple phase clock* to generate a sample value per phase. The multiple phase clock may be generated by a *DLL*. A voted value is determined per phase comprising a majority value of a set of consecutive sample values. *Transition phases* are sensed. A transition phase is defined as two consecutive voted phases comprising different values. The transition phases are compared to a stored phase state to determine a *signal shift direction*. The signal shift direction is filtered to generate a state update signal. The stored phase state is updated based on the state update signal. The stored phase state corresponds to an optimal sampling phase for recovery of the digital signal

(Abstract, Figs.2, 4, 6, 7, 10). The phase selector (#56, #60, Fig.2, Fig.4) comprises a state machine (#126, Fig.6) having five states for shifting the sampling phase toward the optimum phase (Fig.7, Col 6, Lines 58 – 67 to Col 7, Lines 1 - 6).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a state machine to shift the phase state corresponding to the optimal phase for recovery of the digital data. (Col 6, Lines 64 – 67). As discussed earlier, it would have been an obvious matter of design choice to select the number of states of interest.

Re claims 9 and 15, Chen teaches all the limitations of claims 1 and 11, except of the phase detector performing XOR logic operations.

Huang, teaches of the transition phase sensor (#106, Fig.4) as an XOR function (#114, Fig.5). The XOR function detects a 0,1 or a 1,0 sequence in the voted data V(n-1:n). The transition value T_n is set when a transition is detected.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used an XOR logic function for its high speed operation to detect a 0,1 or a 1,0 sequence and set the transition value T_n when a transition is detected.

Claims 10, 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Maddux (US Pub 2003/0061564).

Chen teaches all the limitations of claim 1, 11 and 16 except of a multiplexer coupled to receive the recovered clock and the oversampled data and output the transmitted data.

Maddux, teaches of a data recovery system which comprises of a selector (#208, Fig.2, multiplexer) coupled to receive the recovered clock (from #206) and the oversampled data (from #202) and output the transmitted data (recovered data).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a selector to reliably pass the sample which the decision matrix selects.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristocratis Fotakis whose telephone number is (571) 270-1206. The examiner can normally be reached on Monday - Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AF

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER